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•Good receiver circuits (input buffers) in CMOS chips are required in any high-speed, board-level design to change the distorted signals transmitted between chips (because of the imperfections in the interconnecting signal paths) into well-defined digital signals with the correct pulse widths and amplitudes.

IO Buffers Design - SMDP-C25D

This book is based on a collection of homework problems, design projects and sample interview questions for the VLSI High-Speed I/O Circuits class (EEE598) the author offered in the School of Engineering at Arizona State University. The materials cover various aspects of the design, analysis and application of VLSI high-speed I/O circuits.

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Lecture 23: I/O

– Techniques for High-speed Implementation of Nonlinear Cancellation, Sanjay Kasturia and Jack H. Winters •Overview: – Your project will be the design of a circuit that processes the input data from a high-speed I/O. This processing is generally done in a mixed signal manner today, but your job

Lecture 2 High-Speed I/O - Stanford University

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The materials are organized into twenty-one special topics covering various aspects of analysis, modeling, and implementation of VLSI high-speed I/O circuits, such as prototype timing models, jitter analysis, transmitter, receiver, equalizer, phase-locked loop (PLL), and data recovery circuit designs.

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