

## Iq Calibration Techniques For Cmos Radio Transceivers 1st Edition

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## **On-wafer calibration techniques for giga-hertz CMOS ...**

techniques. When the amount of impairments on the system are  $-4 -2 0 2 4 \times 10^{-4} -4 -2 0 2 4 \times 10^{-4}$  Figure 2. The dashed lines are the decision boundaries for symbols, circles are the ideal symbol locations. known, they can be analytically calibrated by modeling quadrature imbalance and non-linear compression behaviors.

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The design was fabricated in a 0.35- $\mu\text{m}$  CMOS process and dissipates 160 mW from a 3-V supply during on-line calibration, and 95 mW during normal receiving. The die area is 4 mm<sup>2</sup>. View

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## **IQ Mixer Calibration for Superconducting Circuits**

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