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37. The internal cache is loaded with the base address, offset address, and access rights byte 39. The GDTR address the Global Descriptor Table 41.4,096 43. 4M 45. 30000000H 49.

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49. The microprocessor is the controlling element in a computer system. 51. Address bus 53. The I/O read signal causes an I/O device to be read. 55. (a) defines a byte or bytes of memory (b) defines a quadword or quadwords of

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memory (c) defines a word or words of memory (d) defines a doubleword or doublewords of memory

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